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Goddard Space Flight Center

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Stabilization and Control Branch)
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Title: Design of a Digital Command System for the Goddard Rotating Slab Sun Tracker

Principal Engineer: Theodore R. Colburn [1963] 26p info

Introduction

The Goddard Rotating Slab Sun Tracker System is shown in Figure 1 in block diagram form. The digital command system generates a commanded angle, compares it with the angular readout of the digital encoder, computes the digital difference between them, and converts this difference to an analog error voltage. The error signal is the input to the servo drive which changes the position of the rotating glass slab; this change is measured by the digital encoder. Light from the sun is passed through a slit and the resulting beam is refracted by the glass slab. The deflection of the beam from the null point of the detector depends on the angular rotation of the slab, and is measured by the output of the photo-detector upon which the sunlight falls. This output is sent to the satellite attitude control system, which moves the satellite in such a way as to reduce the output of the detector to zero. When the detector is so nulled, the encoder angle is a precise means of measuring the satellite angle in that axis with respect to the sun.

Two types of functions are to be performed by the satellite: offset pointing and raster scan. The offset pointing mode requires that the satellite be made to move at a constant rate and stop when it reaches a predetermined point. This is achieved by increasing or decreasing the commanded angle in each axis at a constant rate until these angles are the coordinates of the offset point. Two types of raster scanning are required: 40 arc-minute square and 5 arc-minute square. Both are achieved by a yaw command which is a triangular function of time with a constant .06 deg/sec rate, and a pitch command which is a series of small, unidirectional steps, occurring when the yaw direction is reversed.

The block diagram of the Digital Command System is shown in Figure 2. The operation of the system is as follows: the diode matrix timer, which consists of a diode matrix connected to a binary counter, produces a sequence of thirty-two pulses. These pulses synchronize the system and establish one comparison cycle. The counter accepts pulses directly from the clock, so the cycle is continuously repetitive. The first sixteen pulses are used to interrogate the encoder. As each track is pulsed, its state is determined and converted to binary form by the gray to binary converter. The converted binary number is shifted into the encoder (difference) register. A command is placed in the command register; this command may be sent from the ground or generated on board as part of a raster scan. The commanded angle in binary form is shifted into a serial subtractor with the encoder number.

OTS PRICE

XEROX

\$

2.60 pl

MICROFILM

\$

0.98 ml

The resulting difference is shifted back into the difference register; it is also passed through a serial comparator circuit to determine whether it is sufficiently large to apply maximum error signal. The difference is then gated into the digital to analog converter to become an error voltage. In the mode of offset pointing a commanded angle is received from the ground and stored; the command register is then counted up or down until it is equal to the commanded angle. Each time the contents of the command and encoder registers are subtracted, the stored command angle and the number in the command register are compared serially in the direction control circuit to establish the counting direction and to determine when the counting is to be stopped.

The system clock rate is derived as follows:
 The sun angle α is related to the slab angle β
 by $5^\circ \alpha = 75^\circ \beta$
 average $\alpha/\beta = 15$

The 16 bit encoder counts 65,536 times per revolution, so

$$75^\circ/360^\circ \times 65,536 = 13,670 \text{ counts in } 75^\circ$$

$$5^\circ \alpha = 18,000 \text{ arc-seconds}$$

so 1 count = $18,000/13,670 = 1.33$ arc-seconds

The raster scan slew rate is to be

$$d\alpha/dt = .06^\circ/\text{second} = 216 \text{ arc-seconds/second}$$

$$216 \text{ arc-sec/sec} \times 1 \text{ count}/1.32 \text{ arc-sec} = 164 \text{ counts/second}$$

Four comparison cycles of 32 clock pulses each occur between each count, so

$$\begin{aligned} \text{clock rate} &= 164 \text{ counts/sec} \times 4 \text{ cycles/count} \times 32 \text{ pulses/cycle} \\ &= 21,000 \text{ pulses/second} \\ \text{clock rate} &= 21 \text{ KC} \end{aligned}$$

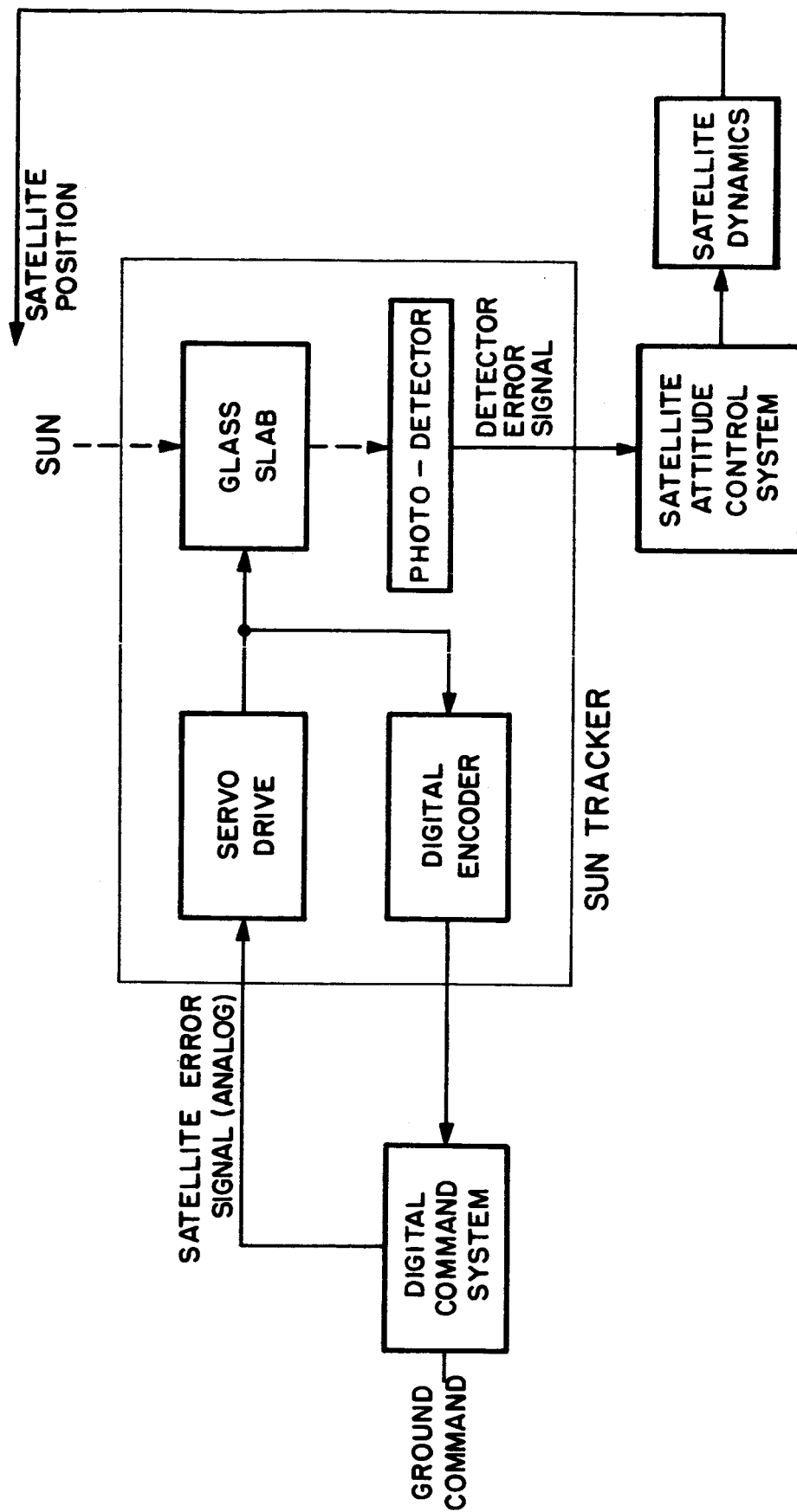
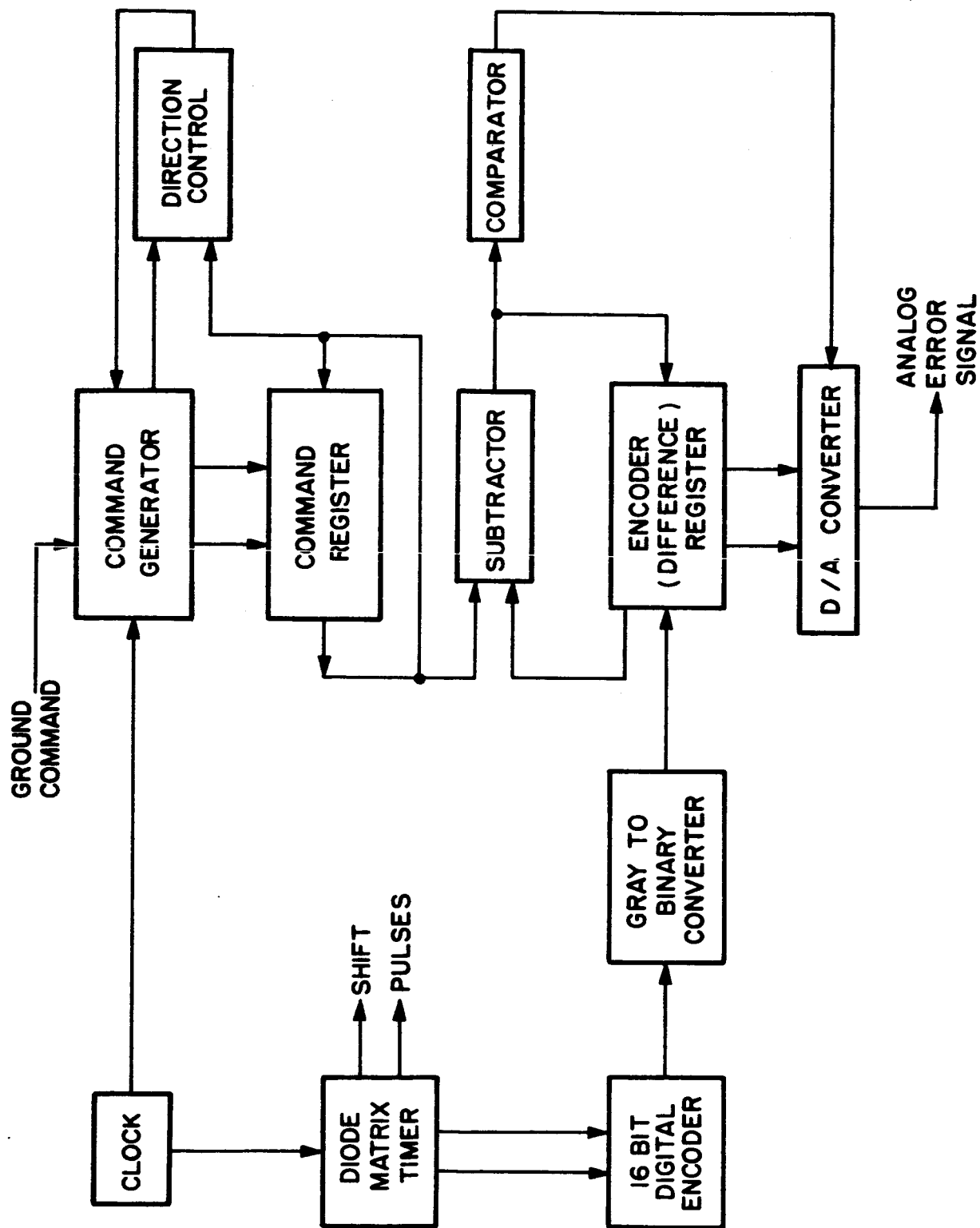


FIGURE 1

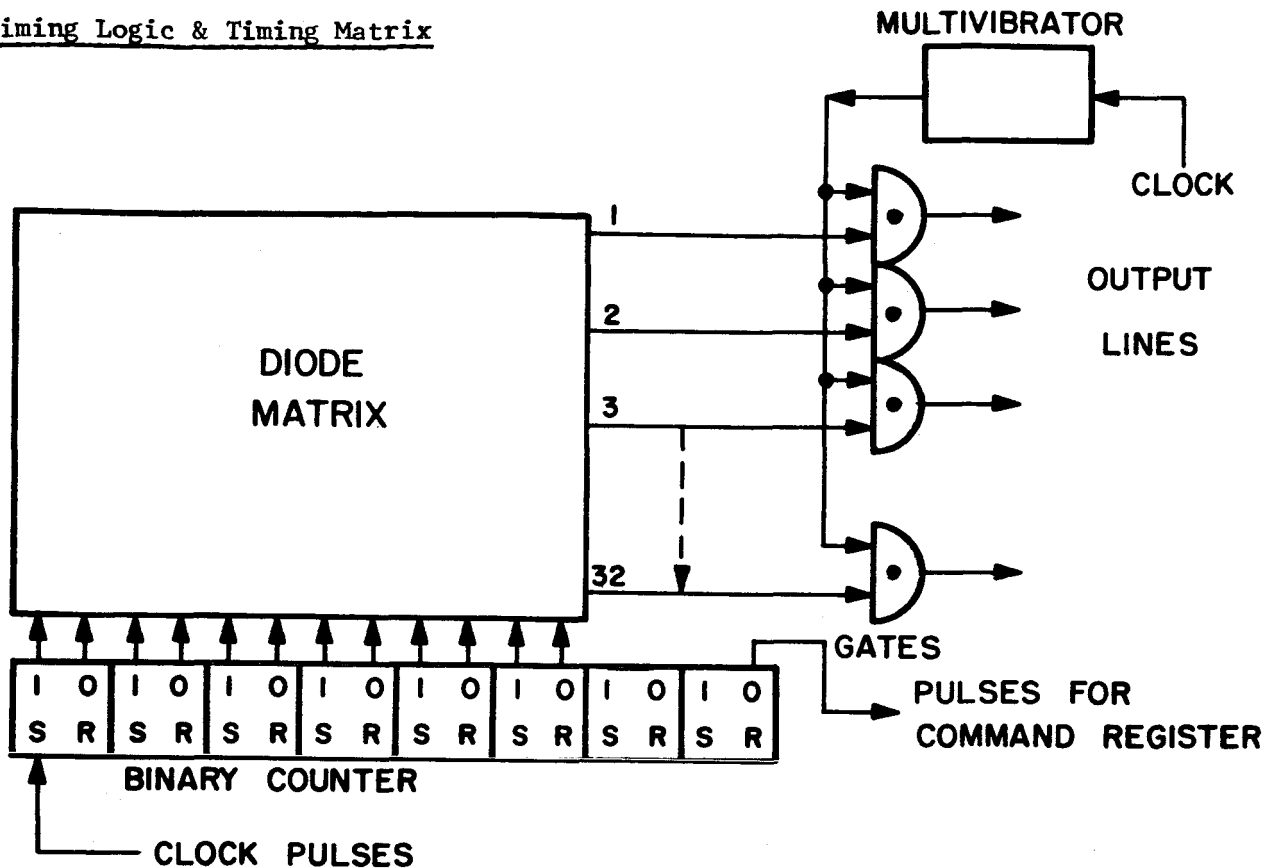
SUN TRACKER SYSTEM



DIGITAL COMMAND SYSTEM

FIGURE 2

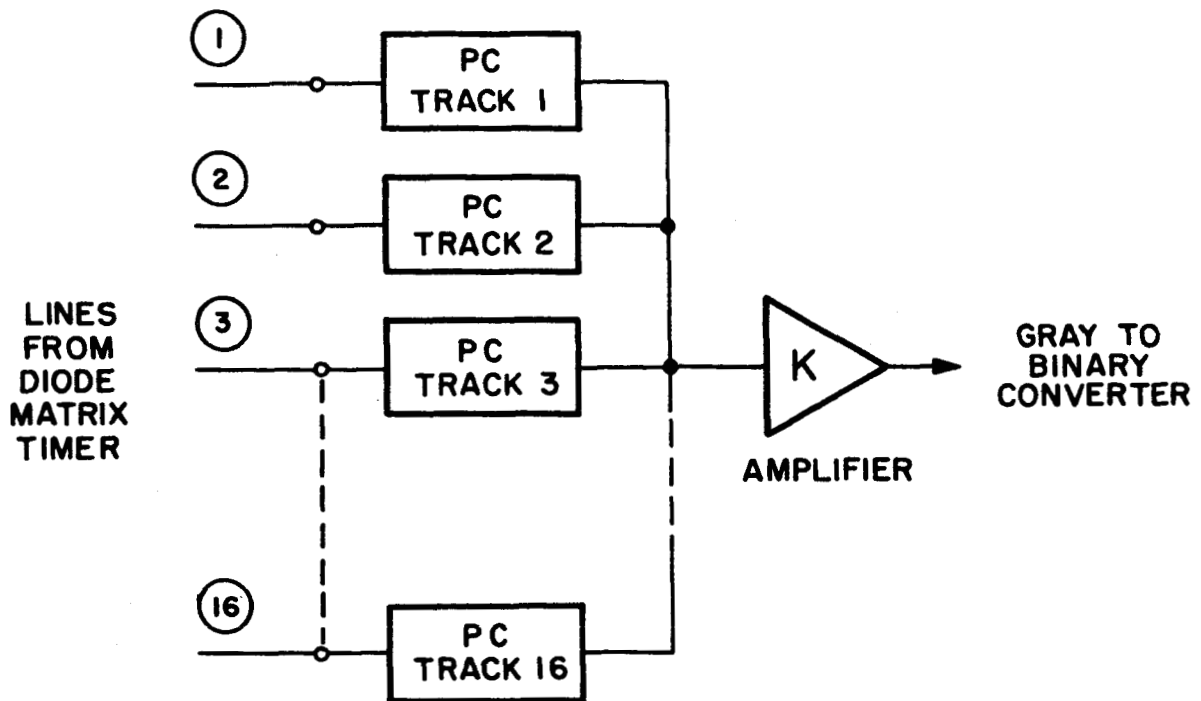
Timing Logic & Timing Matrix



The cycle of the comparison circuit as governed by the cycle of the binary counter. At the beginning of the cycle the counter is set to zero; clock pulses are then fed to the counter. The first pulse sets the counter to a count of one and a pulse is produced on line one; the next pulse sets the count to two and a pulse is generated on line two. The process continues until the maximum count is reached and a pulse is produced on the last line; the cycle is then complete and the counter returns to zero to begin a new comparison cycle. The output lines are sent to various portions of the circuit to perform such functions as interrogation of the encoder and shifting the various registers. The cycle actually consists of 32 clock pulses, provided by the 32 output lines; at the end of the cycle the difference between the command angle and the encoder angle is in the difference register and is being converted to an analog voltage signal.

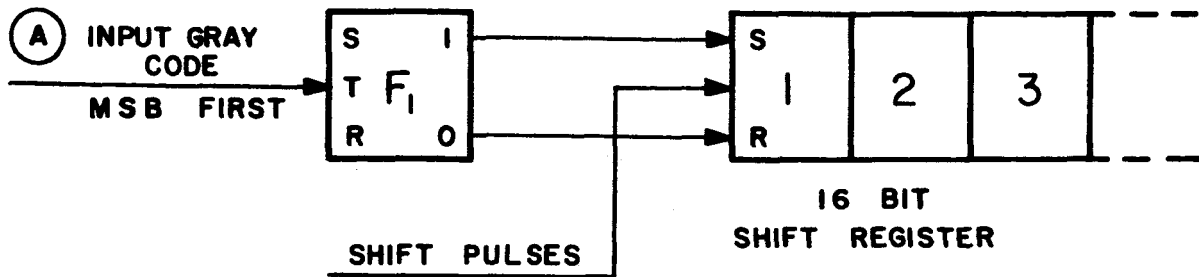
Note that while the portion of the counter connected to the diode matrix returns to zero after 32 pulses, the complete counter requires four such cycles to return to zero. It is the transition of the last stage from one to zero that provides the pulses to count the command register at the scan rate of $.06^\circ/\text{sec}$. The pulses on the output lines are produced as follows: A particular matrix line is set at reference potential by a change in the counter, and the gate of that line is qualified. The same clock pulse which produced this change triggers a monostable multivibrator connected to all the gates. The resultant pulse passes only through the gate which is qualified.

Encoder



The encoder may be represented as shown. Each track of the encoder is a binary bit. A photocell gives the value of the bit as follows: if the cell is illuminated its voltage level allows the circuit in which it is incorporated to pass an interrogation pulse applied to the circuit's input. Thus if a pulse appears on line one from the diode matrix timer, and the photocell is illuminated, the pulse will pass thru, be amplified and shaped, and fed to the gray to binary converter. The pulse would not pass if the cell were not illuminated.

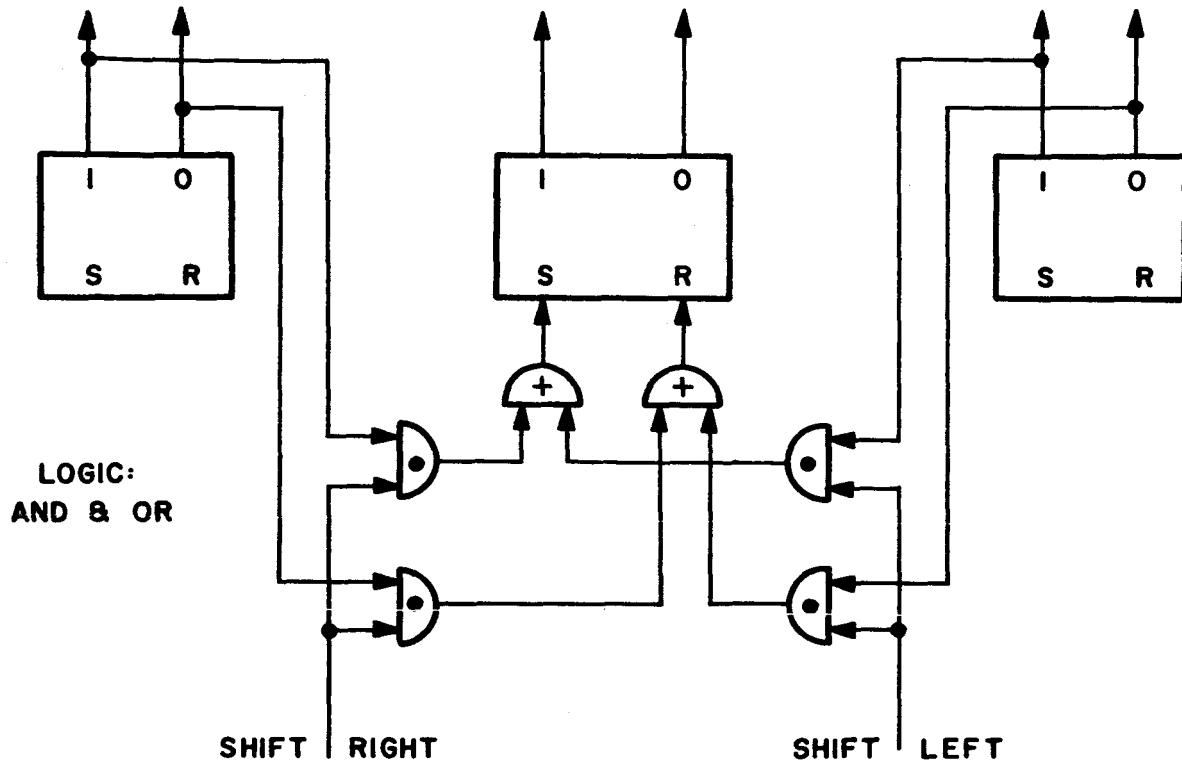
Gray to Binary Conversion



The encoder is interrogated most significant bit first, and the output line (A) is fed into the trigger input of flip-flop F_1 . The output of F_1 is the binary equivalent of the gray coded bit applied to F_1 's trigger input. F_1 is initially set to zero before the encoder is interrogated. The theory of conversion is as follows: The first gray "one" produces a binary "one". The next gray bit is compared with the preceding binary bit; if they are similar the corresponding binary bit is a "zero"; if they are dissimilar, the binary bit is a "one". This is the operation of the configuration shown; the first gray "one" triggers the flip-flop to "one"; if the next gray bit is "zero", F_1 is unchanged and the binary bit is "one"; if the gray bit is "one" F_1 is triggered to the zero state and the resulting binary bit is "zero".

The output of the converter is fed into a 17 stage shift register called the encoder register. The first interrogation pulse applied to the encoder produces an answer which is the state of the most significant bit of the encoder; this answer is registered in F_1 and its binary equivalent is set into stage 1 of the encoder register. The whole process occurs in the time following the first pulse and is completed before the second pulse appears. The second pulse interrogates track 2 of the encoder and also shifts the bit in stage 1 of the encoder register to stage 2. Thus it requires 16 pulses to totally interrogate the encoder and store the converted number in the encoder register; the first 16 pulses of the timing matrix will be used for this function.

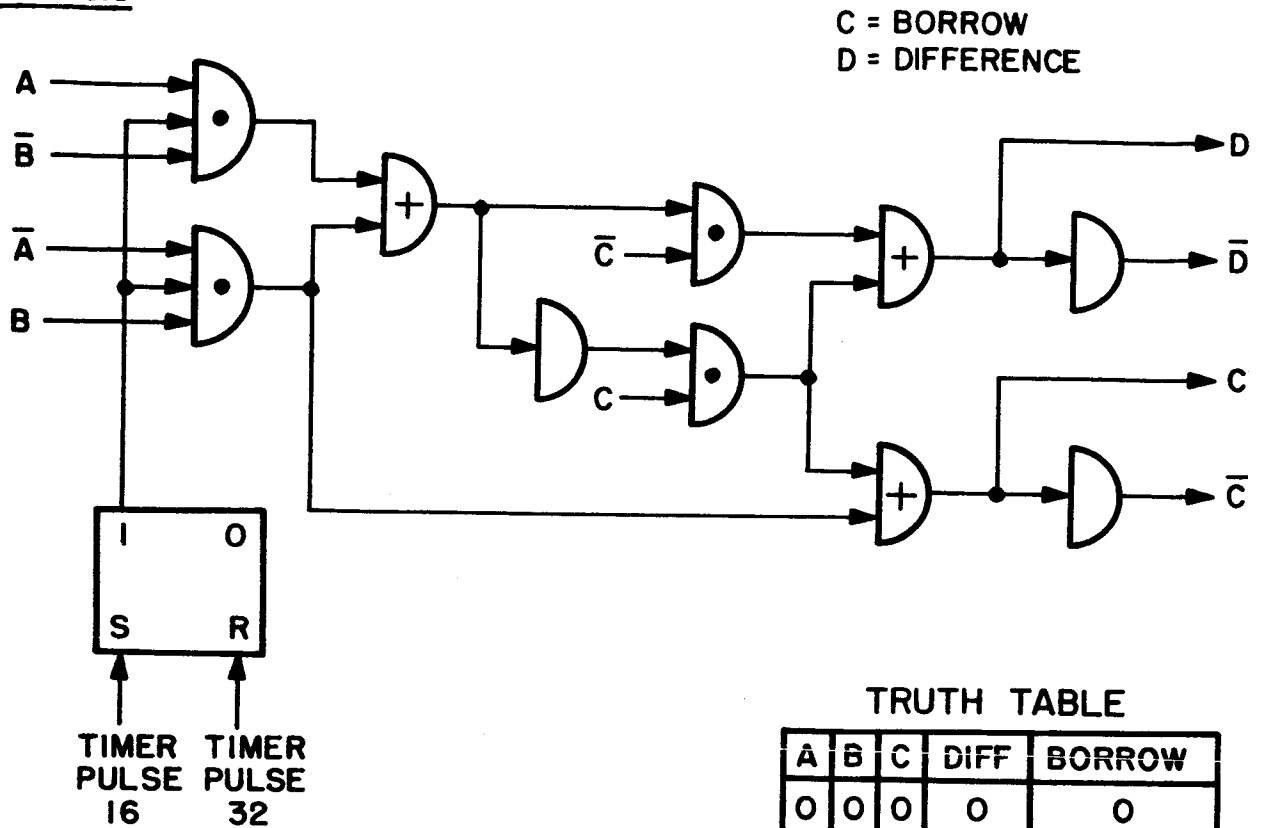
N Register (Encoder Register)
(Difference Register)



The N Register stores the converted binary encoder angle and then the difference between this angle and the commanded angle. The encoder is interrogated track by track, each bit converted from gray code to binary and shifted left to right into the N Register. The next step is to shift the angle into the subtracter; however the angle came from the encoder most significant bit first and the subtraction logic requires that the angles be introduced least significant bit first. Hence the shift into the subtracter must be right to left out of the N Register; the register must then be equipped to shift right or left. The logic of a single stage of such a register is shown. The register need never be reset to zero because the encoder angle, when shifted in, will force out the old difference angle and the new difference angle will follow the encoder angle as the latter is shifted out.

Although both the encoder number and the difference number are 16 bits, the register is 17 bits; the added stage stores the sign associated with the difference number.

Subtractor



LOGIC EQUATIONS

$$\text{DIFF} = (\bar{A}\bar{B} + \bar{A}B)\bar{C} + (AB + \bar{A}\bar{B})C$$

$$\text{BORROW} = (AB + \bar{A}\bar{B})C + \bar{A}B$$

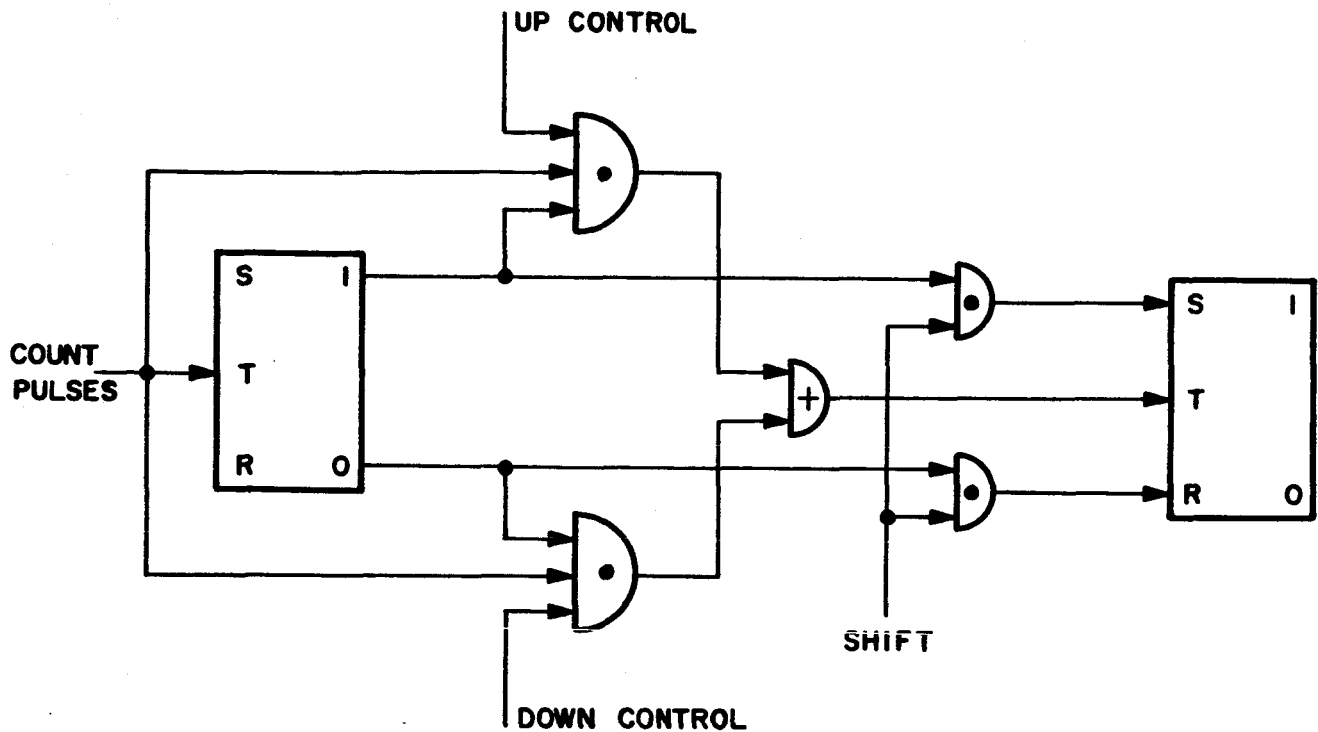
A = MINUEND
 B = SUBTRAHEND
 C = BORROW INPUT

TRUTH TABLE

A	B	C	DIFF	BORROW
0	0	0	0	0
0	1	0	1	1
1	0	0	1	0
1	1	0	0	0
0	0	1	1	1
0	1	1	0	1
1	0	1	0	0
1	1	1	1	1

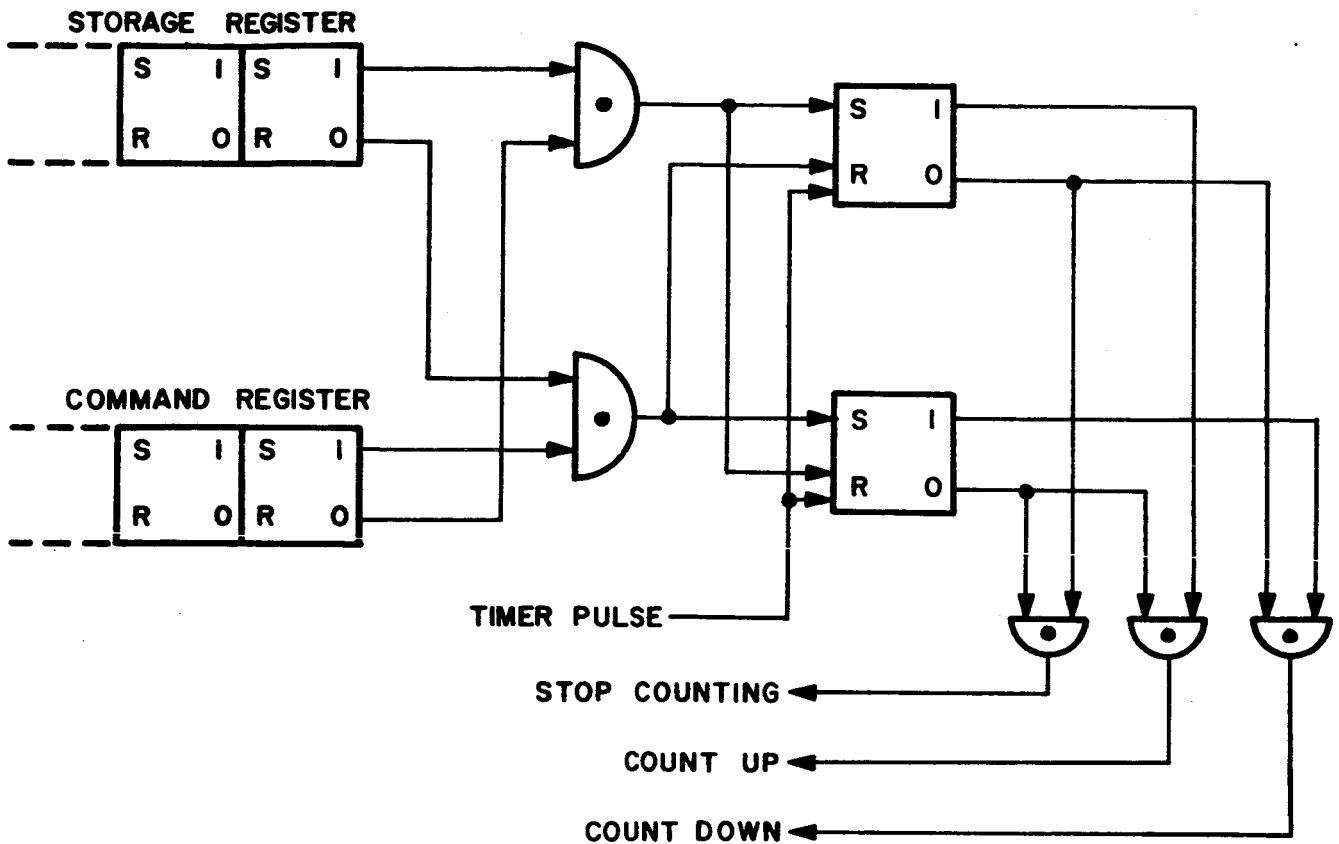
The truth table of serial subtraction yields the logic equations shown. When A is larger than B the difference will be in straight binary form; if B is larger the difference will be in two's complement form. When two sixteen bit numbers are subtracted the seventeenth bit of the difference is an indication of the form of representation: Zero is binary and one is two's complement. The subtractor is made operable by qualifying the input gates with pulse 16 of the timer.

Command Register



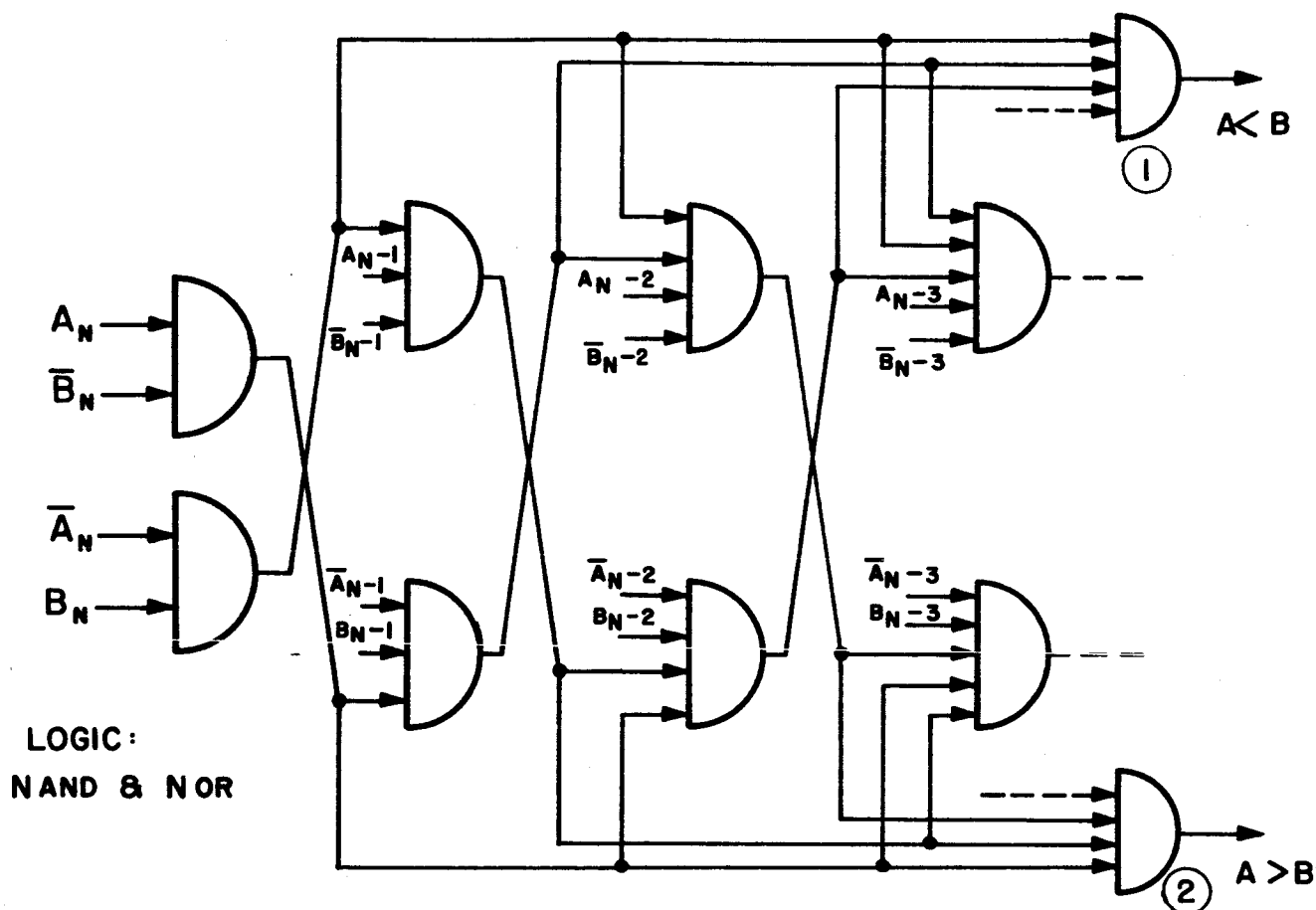
The command register stores the binary representation of the commanded angle. This angle is shifted out to be subtracted from the encoder angle so the register must have uni-directional shifting capability. During both the raster scan and the offset pointing modes the command is required to increase or decrease at a constant rate; thus the register must be an up-down counter as well. One stage of such a register is shown above.

Count Direction Control (Serial)



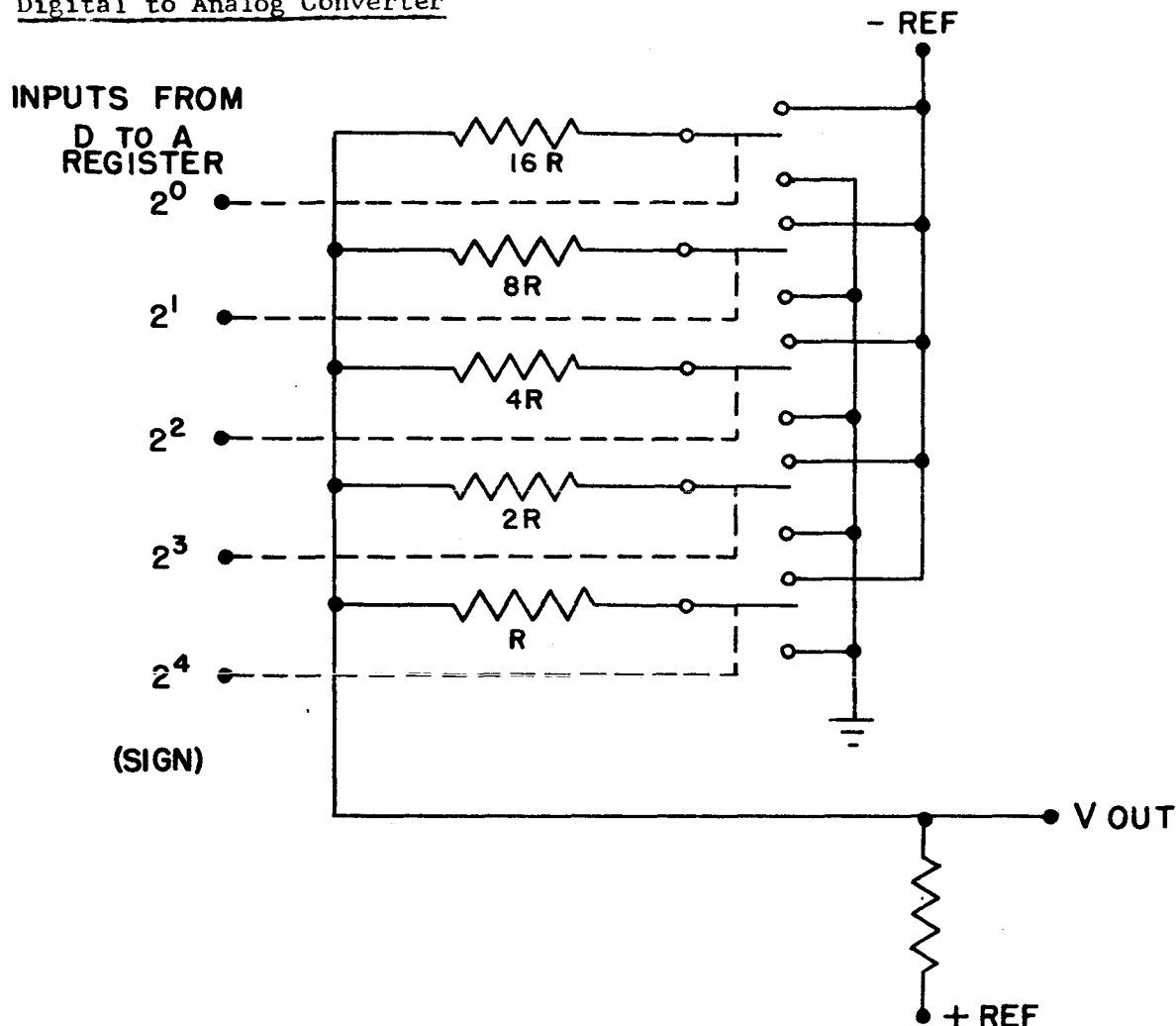
The offset pointing mode requires that the spacecraft move to the desired point at a constant rate. The commanded point is placed in a storage register; each time the contents of the command register are subtracted from the encoder angle they are compared with the offset point through the serial comparator shown above. The comparator is inspected after the shifting has been completed; the two flip-flops now represent the most significant differing bits of the two registers. If both flip-flops are in the zero state after the numbers are compared, the counting of the command register is stopped because the offset point has been reached. During raster scan the command register is counted up and down independently, and no number is stored in the storage register. The comparison mentioned above is performed during raster scan, but the three outputs shown in the figure are gated shut so as to have no effect on the system.

Comparator



The first four stages of an N stage parallel comparator are shown. The operation is from left to right; if $A_N = B_N$ the comparison moves to the next stage; if $A_N = 1$ and $B_N = 0$ then $A > B$ and is noted by an output at gate two. Once a stage is reached where $A_K \neq B_K$ an output is recorded on either of gates (1) or (2) and this output is unaltered by further comparison of later stages. The maximum comparison time is $(N + 1)$ times the delay of the gates.

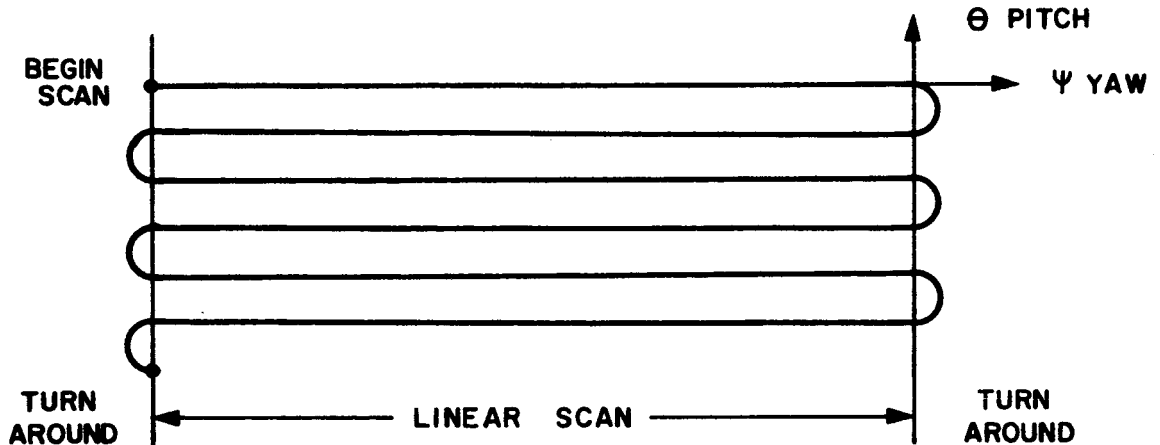
Digital to Analog Converter



The digital to analog converter is a bipolar type employing transistor switches and a resistive ladder. The output voltage is positive for numbers in straight binary form and is negative for numbers in two's complement form. The commanded angle is considered the minuend and the encoder angle the subtrahend. When the subtrahend is greater than the minuend the resulting difference is in the two's complement form; the difference is in straight binary form if the minuend is greater than the subtrahend. The most significant bit input of the converter is taken from the sign stage of the encoder (difference) register; the sign determines the representation of the number.

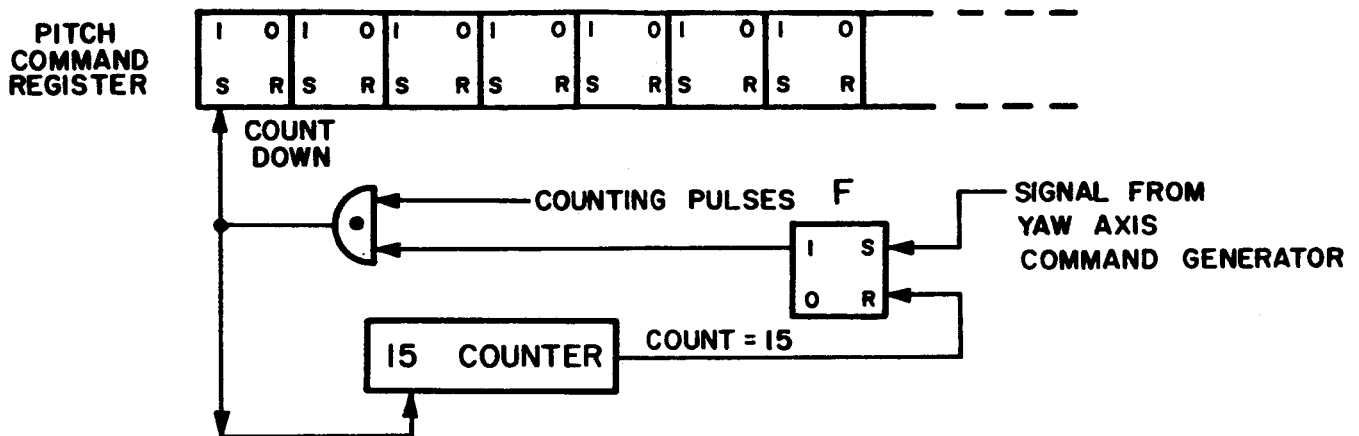
The converter consists of five transistor switches each having two positions which are governed by the state of each stage of the D to A register. In one position the switch connects its resistor with the negative reference, allowing current to flow; the other position is to ground and no current flows. The output is floated by the positive reference, so that bipolar operation is possible.

Raster Scan



The raster scan pattern is divided into two sections: Linear scan and turn around. During the linear portion the pitch position angle θ is held constant while the yaw angle ψ is increased or decreased at a constant rate. During turn around the pitch angle is decreased at a constant rate while the rate of change of yaw angle decreases from a constant value of $+V_0$ to zero and then increases to $-V_0$. The scan is accomplished by counting the command registers up or down with pulses issued at the proper rate by the pitch and yaw axes command generators. The length of a scan line is either 40 minutes or 5 minutes. The angle θ between lines is 20 seconds. The maximum time allowed for turn around is 3.9 sec. time; the design in this report employs a turn around time of 3.6 seconds.

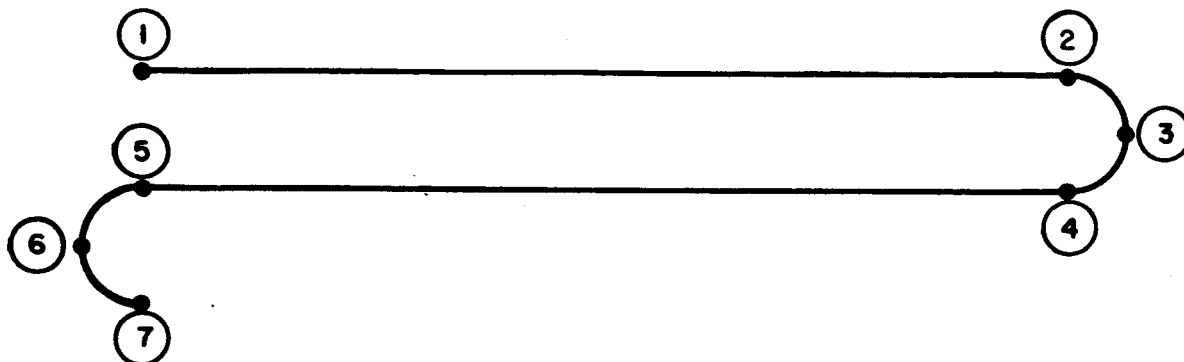
Pitch Axis Command Generator



The pitch command generator is quite simple. The flip-flop F is set to state "one" by a signal from the yaw axis command generator indicating the linear scan line is complete. The flip-flop qualifies the "and" gate and allows the counting pulses to pass. These pulses are frequency-divided pulses from the master clock and occur at intervals of 3.6/15 seconds. That is, 15 pulses will decrease θ the necessary 15 seconds; since the rate of decrease must be constant and turn around time is 3.6 seconds time, the pulse rate is that given. The pulses are fed both to the command register and to a counter which indicates when 15 pulses have passed, at which time the flip-flop is reset and the gate is closed, allowing no more pulses to pass. The cycle is repeated when the next linear scan line is completed.

Yaw Axis Command Generator

The yaw axis command generator is far more complex than the pitch axis command generator. Define a cycle of yaw axis raster scan as follows:



The cycle begins at point (1). From (1) to (2) the command register is counting up at a constant linear rate. Point (2) is the start of turn around; the register counts up at a decreasing and non-linear rate until (3). From (3) to (4) the register counts down at an increasing and non-linear rate. From (4) to (5) the register counts down at a constant rate, the same rate as from (1) to (2). Point (5) is the start of the next turn around; from (5) to (6) the register counts down at a decreasing rate; from (6) to (7) it counts up at an increasing rate. Point (7) completes the cycle.

The function of the command generator is to provide the counting pulses at the proper rates and to set the register for up or down counting. The logic is as follows: The command to raster scan is given, so the register is set to count up. Frequency divided counting pulses are accepted from the master clock and the register counts up at a constant rate. The pulses are counted by a separate counter until enough have passed to bring the spacecraft to position (2). At this point the clock pulses are stopped and counting pulses are accepted from the turn around generator, which is to be explained below. When point (3) is reached the turn around generator sends out a signal which sets the register to count down. When point (4) is reached control is again transferred and the register accepts clock pulses once again. The rest of the cycle is analogous.

The counting pulses for the yaw axis command generator occur at a frequency of 164 pulses per second.

The yaw axis command generator is shown in Figure 6.

Turn Around Generator

The equation of the yaw axis position during turn around is of the form

$$(1) \quad Y = -\frac{1}{2} a t^2 + V_0 t$$

V_0 is the velocity of scan or the rate of angle increase and is $V_0 = 216$ steps/sect. If we constrain the turn around time to be $T_{\text{turn}} = 3.6$ sect, then V , the yaw axis velocity, would be zero at $t = 1.8$ sect. Then

$$(2) \quad \begin{aligned} a &= -164 \text{ steps/sect.} / 1.8 \text{ sect.} \\ a &= -90 \text{ steps/sect.}^2 \end{aligned}$$

Equation (1) is now

$$Y = -\frac{1}{2} (90 \text{ steps/sect}^2) t^2 + (164 \text{ steps/sect.}) t$$

$$(3) \quad Y = -45 t^2 + 164 t$$

The differential is

$$dY = -90 t dt + 164 dt$$

$$(4) \quad dY = dt (-90 t + 164)$$

dt is constrained to be the counting pulse period, and t is the summation of all preceeding dt . The command register is to be advanced by one pulse (an increase in yaw angle of 1.33 seconds) whenever

$$Y_N - Y_{N-1} \geq 1.33 \text{ seconds} = \Delta Y$$

Y_N and Y_{N-1} are determined by equation (3).

To implement the equation digitally in the most simple manner, equation (4) will be approximated by:

$$(5) \quad dY = dt (-128t + 227)(3/4)$$

If the dt (clock pulses) are counted in a binary counter the total count at any time will be T . Shifting t left seven bits will be $128t$.

$$dY = 0 \text{ when } t = 227/128$$

$$\begin{aligned} \text{At this time the count in the register will be count} &= t/dt \\ &= 227/128 dt \end{aligned}$$

But $dt = 1/164$ sect

$$\begin{aligned} \text{So count} &= (164)(227)/128 \\ \text{count} &= 228 \end{aligned}$$

$$\begin{aligned} \text{So } 128t &= 227 \text{ and } t = 288 \\ \text{then } 227 &= 128 (288) \text{ in register} \end{aligned}$$

It may now be seen that

$$(6) \quad dY = dt (-128t + (128)(288)(3/4))$$

$$(7) \quad 4/3 dY = 128 dt (-t + 288)$$

Thus if the register count t is subtracted from 288, dY is determined because dt is unity in the register and a factor of 128 is merely a shift of seven bits.

$$\text{Now } (8) \quad 4/3 dY = 288 - t$$

Theoretically the register should be advanced by $\Delta Y = 1.33$ second whenever $\sum dY \geq 288$. In this case simplicity and a better approximation to the ideal curve are obtained by advancing the command register whenever $\sum dY \geq 224$.

Counting dt in a register and subtracting from 288 is equivalent to counting down from 288. The process is now as follows: Turn around is begun by inserting the binary equivalent of 288 in a register. The first counting pulse appears and counts the register down to 287. This number is compared with 224 and if found to be greater, so a pulse is produced which advances the command register by one unit. This operation continues until the counter is down to 223; this number is not ≥ 224 so it is stored in another register. No pulse is fed to the command register. The next dt pulse counts the register down to 222 and this number is added to the 223 that was stored. Their sum is compared with 224, and found to be greater. So a pulse is fed to the command register and the storage register is cleared. The operation is then repeated.

In general: the counter is counted down by a dt pulse; this new number is added to the contents of the storage register. If their sum is less than 224 it is stored. If it is greater than 224 a pulse is fed to the command register and the storage register is cleared.

When the counter reaches zero, this is the midpoint of turn around. The dt pulses are now counted up in the counter and the second half of turn around is a replication of the first half.

The ideal turn around curve is a parabola of the form of Equation 1. The pattern generated by the method just described is an approximation generated by a series of straight lines of changing slopes. The approximation is quite close in the critical areas of the turn around, the beginning, midpoint, and end, and is within 19 arc-seconds of the ideal curve at its maximum deviation point.

The turn around generator is shown in Figure 7.

The system operation will now be described in detail. The pulses from the diode matrix are distributed as follows: Pulses 1 through 16 are used to trigger monostable multivibrators in each track of the encoder; these multivibrators form the pulses of the proper shape to interrogate the encoder. Pulses 2 through 16 are used to shift the encoder register and the gray to binary converter. Lines 2 through 16 are then gated to a common output line called the shift right line. Pulses 17 through 32 are similarly gated to a common line called the shift left line; this line shifts the encoder register and the command register through the subtractor, the difference back into the difference (encoder) register, and the command and storage register through the direction control circuit. Individual pulses will be used to perform various system functions as will be explained below.

Formation of these pulses is achieved as follows. The binary counter accepts pulses from the clock; at a particular count one of the output lines of the diode matrix will be at reference potential while the rest are at ground potential. The monostable multivibrator which strobes all the gates simultaneously is triggered by the same pulses accepted by the counter; thus the inherent delay in the output pulse of the multivibrator allows the matrix to settle and the proper gate to be qualified before the pulse which is to be gated arrives. The total transition time of the multivibrator must obviously be less than the clock period so that each clock pulse triggers a new transition cycle.

An interface matching problem may occur between the encoder output pulses and the gray to binary converter if microminiature circuits are used; that is, the amplitude of the encoder output pulse may be too great to be compatible with the input requirements of the low voltage circuits. The use of a Schmitt Trigger whose output pulse is of the proper magnitude to be compatible is then necessary.

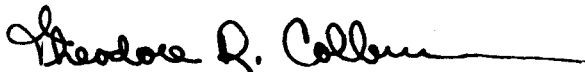
The first timer pulse interrogates the first (most significant) track of the encoder; an encoder output pulse is produced which is converted to a compatible pulse by the Schmitt Trigger and converted to binary form by the gray to binary converter. The flip-flop of the converter is fed through gates which have previously been opened to the first stage of the encoder register; thus before the second timer pulse arrives the first bit of information has been stored. The sixteen bits of encoder angle will be completely stored in the encoder register after sixteen interrogation pulses and fifteen shift pulses. No information is presently in the 17th stage of the encoder register. However, between the 16th and 17th timer pulses the least significant bits of the encoder and command registers are being subtracted and the first difference bit is in the 17th stage of the encoder register. The inputs to the subtracter are opened and closed by the timer so that the subtracter is operative only during the subtraction process. Completion of the sixteen bit subtraction plus the seventeenth (sign) bit requires sixteen shift pulses; timer pulses 17 through 32 are used. The

difference angle must now be gated into the D to A register before the first pulse of the new cycle, which begins to place a new encoder reading in the encoder register. The gates are opened on the 32nd pulse and closed on the first pulse of the new cycle. The time delay of opening the gates will be sufficient to allow the final shift of the encoder register to take place, and the gates will be closed before the first bit of the new number reaches the register, so the number which is gated into the D to A register will be the correct one at all times.

The desired analog voltage characteristic is shown in Figure 3. Logic is required to provide that full analog voltage is applied if the digital difference is greater than 16 units (16 times the value of the least significant bit). The comparator circuit shown in Figure 4 performs this logic. After the first four least significant bits have passed through the subtracter, its output is gated through the serial comparator. If all the bits remaining are zeros, the logic determines that the difference is in straight binary form and is not greater than 16, so the output of the subtracter is gated into the D to A converter. If all the bits remaining are ones the difference is in two's complement form and is also not greater than 16, so again the subtracter output is gated into the D to A converter. If all the remaining bits are not of the same sign then the absolute value of the error is greater than 16, so the D to A converter must be driven to its maximum output voltage. This is done by inserting all ones in the converter if the representation is straight binary and all zeros if the representation is two's complement. The comparator shown within the dashed lines may be replaced by the parallel comparator of Figure 5 minus, of course, the difference register. The advantages of the parallel comparator are: four modules rather than five if integrated microcircuits are used, and less chance of error in the logic. The disadvantage is many more connections between modules. The parallel comparator is more desirable if high reliability of connections can be assured.

The offset pointing mode is more efficient when rate limiting is employed because large overshoots are avoided. When rate limiting is not used, the commanded angle is placed in the storage register and is gated directly into the command register, rather than allowing the latter to count up or down until it reaches the commanded angle. Thus the error between the encoder angle and the commanded angle would jump immediately to a large value. The response time of the sun tracker system would drive the slab to the commanded angle quickly, while the such slower response of the spacecraft causes a large error voltage from the detector, and for large offset commands the sun line may be driven out of the field of view of the detector. Assuming the sun line remains in the field of view of the detector, the spacecraft will build up a large rate and will overshoot the offset point. The error voltage will then reverse and drive the spacecraft back toward the offset point; an overshoot in the reverse direction may also occur. Such overshooting is undesirable in that additional power is consumed in stabilizing the spacecraft once the offset point is reached; the rate limited mode previously described is more efficient in this respect.

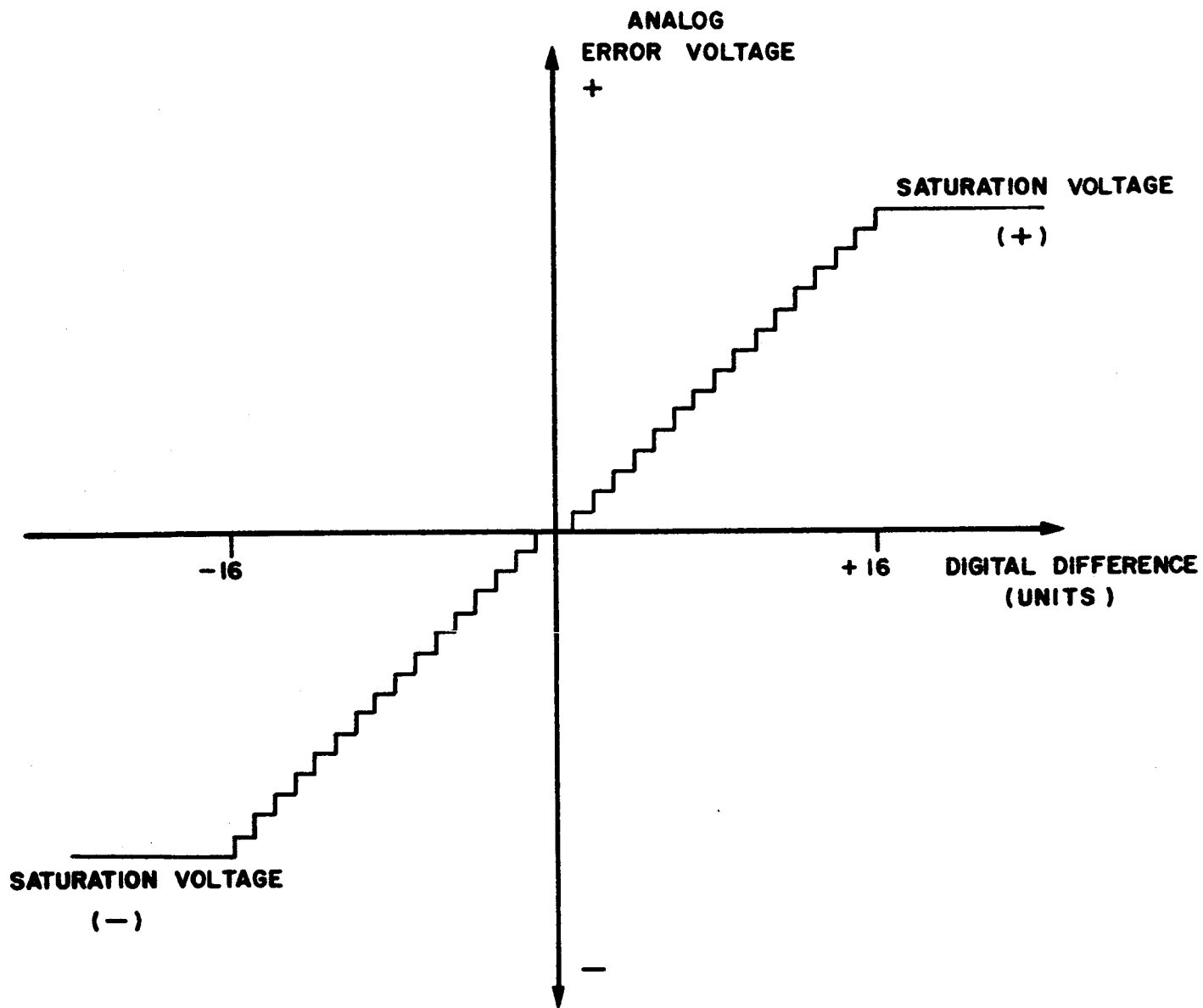
A capability for both modes of offset pointing would require direct gating from the outputs of each stage of the storage register to the inputs of the corresponding stage of the command register. The gates would be qualified by a pulse from the timer, so the angle in the storage register would be gated into the command register once each comparison cycle. The pulse would not be applied if the rate limited mode is used.



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**DIGITAL ERROR
VS.
ANALOG ERROR VOLTAGE**

FIGURE 3

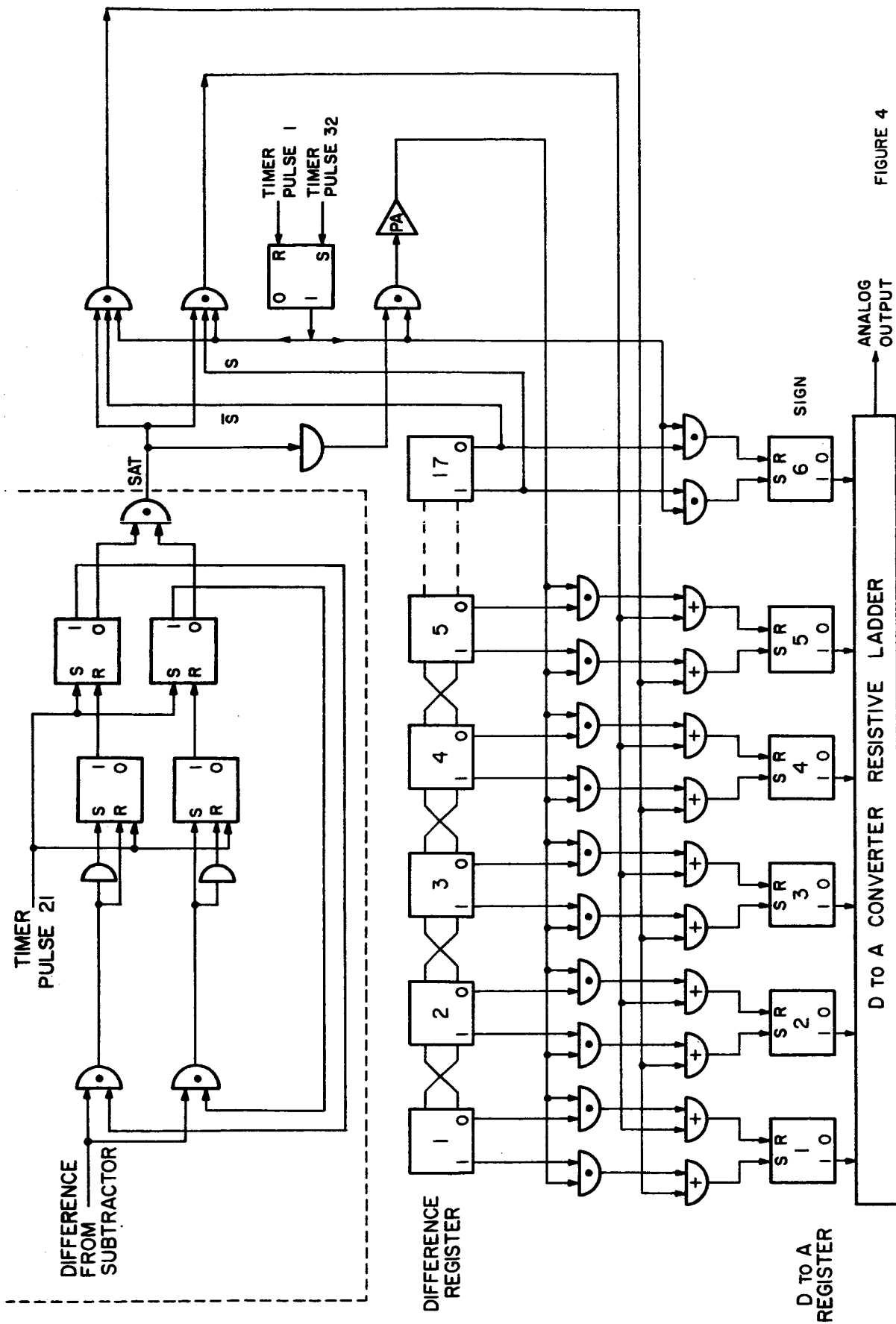
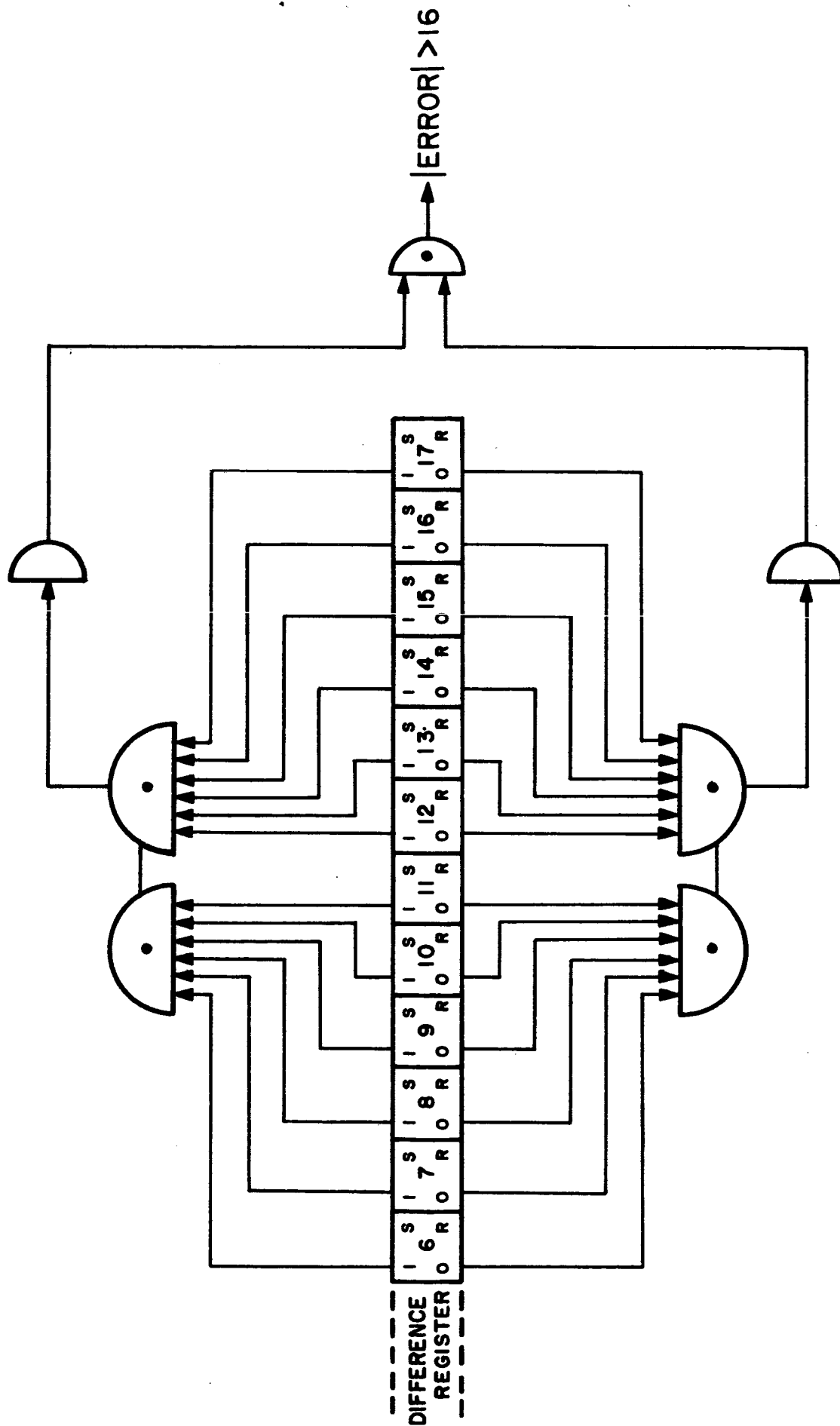


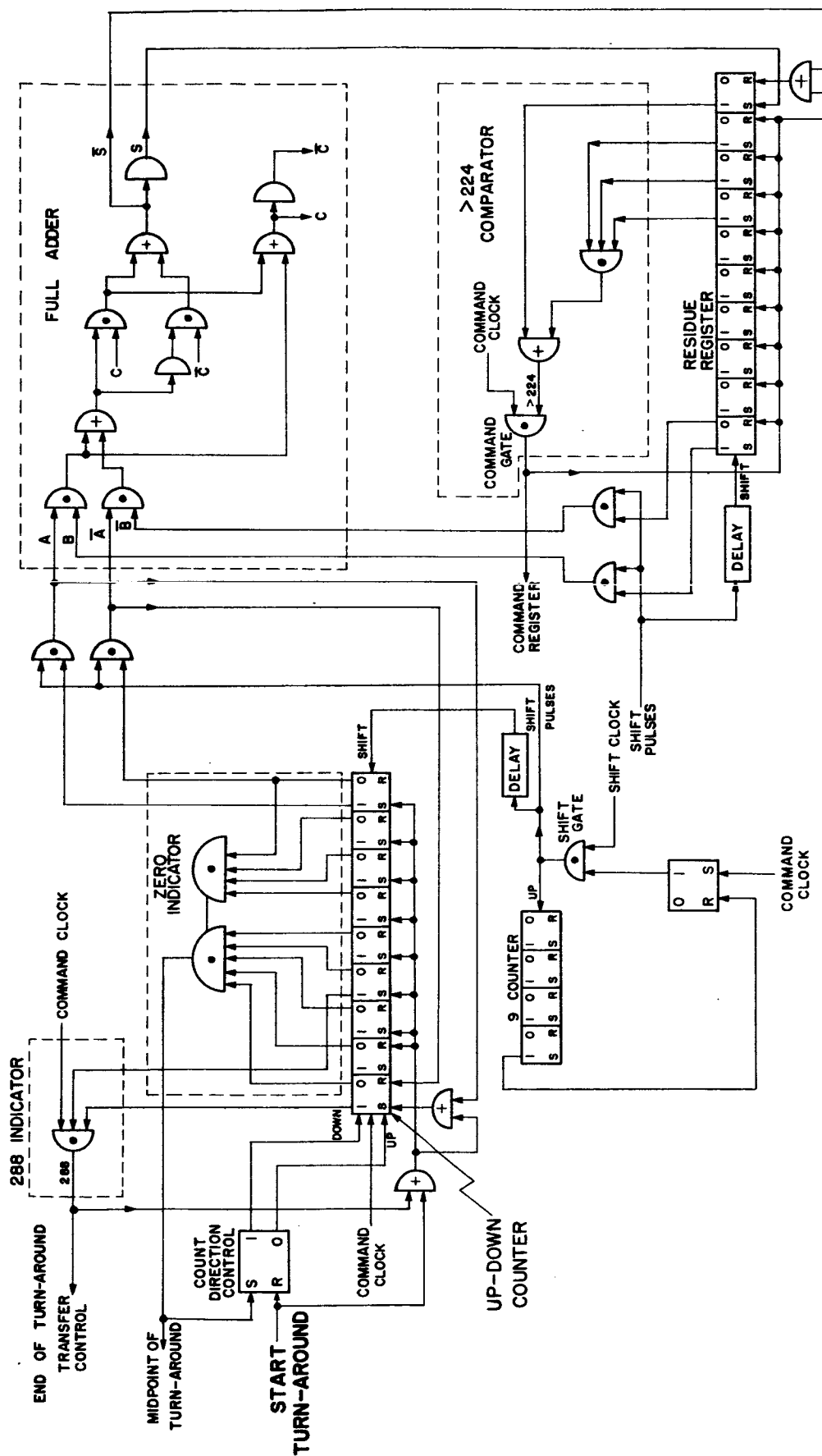
FIGURE 4



ALTERNATIVE COMPARATOR



6



YAW AXIS TURN-AROUND GENERATOR